In the Claims:

Please amend the claims as indicated below:

1-5. (canceled)

6.(currently amended) A ~~redundant single event upset suppression system,~~ system comprising:

~~at least two semiconductor registers logically connected and each including CMOS~~ transistors adapted to operate as ~~a logical cross-coupled Nor Gate~~an SR flip-flop~~; and~~

~~inputs to the register comprised of CMOS gates acting as insulators~~ wherein each one of the transistors has an insulated gate and wherein the SR flip-flop is a SEUSSNor comprising:

a power node and four p type transistors named P2, P4, P6, and P8 wherein the sources of P2, P4, P6, and P8 are connected to the power node;

a ground node and eight n type transistors named N1, N2, N3, N4, N5, N6, N7, and N8 wherein the sources of N1, N2, N3, N4, N5, N6, N7, and N8 are connected to the ground node;

a p type transistor called P1 wherein the source of P1 is connected to the drain of P2;

a p type transistor called P3 wherein the source of P3 is connected to the drain of P4;

a p type transistor called P5 wherein the source of P5 is connected to the drain of P6;

a p type transistor called P7 wherein the source of P7 is connected to the drain of P8;

an S input connected to the gate of P1, the gate of N1, the gate of N5 and the gate of P5;

an R input connected to the gate of P3, the gate of N3, the gate of N7 and the gate of P7;

a Q2 node connected to the gate of P2, the gate of N6, the drain of N7, the drain of P7, and the drain of N8;

a Qbar node connected to the gate of P4, the gate of N8, the drain of N1, the drain of P1, and the drain of N2;

a Q node connected to the gate of P6, the gate of N2, the drain of N3, the drain of P3, and the drain of N4; and

a Qbar2 node connected to the gate of P8, the gate of N4, the drain of N5, the drain of P5, and the drain of N6.

7-10.(cancelled)

11.(currently amended) A ~~single event upset suppression system,~~ system comprising:

~~at least two semiconductor registers logically connected and each including CMOS~~ transistors adapted to operate as ~~a logical cross-coupled Nor Gate~~an SR flip-flop~~; and~~

~~inputs to the register comprised of CMOS gates acting as insulators~~ wherein each one of the transistors comprises has an insulated gate and wherein the SR flip-flop is a SEUSSNand comprising:

a power node and eight p type transistors named P1, P2, P3, P4, P5, P6, P7, and P8 wherein the sources of P1, P2, P3, P4, P5, P6, P7, and P8 are connected to the power node;

a ground node and four n type transistors named N2, N4, N6, and N8 wherein the sources of N2, N4, N6, and N8 are connected to the ground node;

an n type transistor called N1 wherein the source of N1 is connected to the drain of N2;

an n type transistor called N3 wherein the source of N3 is connected to the drain of N4;

an n type transistor called N5 wherein the source of N5 is connected to the drain of N6;

an n type transistor called N7 wherein the source of N7 is connected to the drain of N8;

an S input connected to the gate of P1, the gate of N1, the gate of N5 and the gate of P5;

an R input connected to the gate of P3, the gate of N3, the gate of N7 and the gate of P7;

a Qbar2 node connected to the gate of P2, the gate of N6, the drain of P7, the drain of N7, and the drain of P8;

a Q node connected to the gate of P4, the gate of N8, the drain of N1, the drain of P1, and the drain of P2;

a Qbar node connected to the gate of P6, the gate of N2, the drain of N3, the drain of P3, and the drain of P4; and

a Q2 output node connected to the gate of P8, the gate of N4, the drain of N5, the drain of P5, and the drain of P6.

12-15.(cancelled)

16.(new) The system of claim 6 further comprising at least two more SR flip flops and a voting circuit such that the circuit output is the majority output of all of the SR flip-flops.

17.(new) The system of claim 16 wherein the voting circuit is a TRed2 circuit.

18.(new) The system of claim 6 further comprising at least two more SR flip flops and a correction circuit such that the circuit output is the corrected output of all of the SR flip-flops.

19.(new) The system of claim 18 wherein the voting circuit is a TRed1 circuit.

20.(new) The system of claim 11 further comprising at least two more SR flip flops and a voting circuit such that the circuit output is the majority output of all of the SR flip-flops.

21.(new) The system of claim 20 wherein the voting circuit is a TRed2 circuit.

22.(new) The system of claim 11 further comprising at least two more SR flip flops and a correction circuit such that the circuit output is the corrected output of all of the SR flip-flops.

23.(new) The system of claim 22 wherein the voting circuit is a TRed1 circuit.

24.(new) A system comprising:

three registers having the functional behavior of an SR flip-flop; and

a correction and feedback circuit that accepts the outputs of the three registers, produces a corrected output, and returns a signal to the inputs of the three registers.

25.(new) The system of claim 24 wherein the feedback and correction circuit is a TRed1 circuit comprising:

26.(new) The system of claim 24 wherein the feedback and correction circuit is a TRed2 circuit comprising:

27.(new) The system of claim 24 wherein at least one of the three registers is a SEUSSNor.

28.(new) The system of claim 24 wherein at least one of the three registers is a SEUSSNand.